ABSTRACT OF THE DISCLOSURE

A system and method are presented for indicating active tag bits within valid entries of a dual-clock FIFO data buffer, used to transfer data between two clock domains. Data (containing tag bits) are written to the FIFO and read from the FIFO using separate clocks. Data writes are synchronous with the first clock, while reads are synchronous with the second clock. A FIFO entry is "valid" after data has been written to it, and before it is read. The system disclosed herein identifies the valid FIFO entries and generates a set of logic outputs, synchronized to the second clock (i.e., the read clock). Each output corresponds to one of the tag bit positions, and is HIGH if the corresponding tag bit is HIGH in any of the valid entries. This creates a means of detecting active tag bits in the FIFO without having to actually read each entry. Since the tag bits convey important information about the source and nature of the data, this detection system may expedite the data transfer. A simple implementation of the method is described, based primarily on conventional combinatorial logic. The method is straightforward and can readily be incorporated into an integrated circuit.